IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Claim 1 (Original): A pressure contact type semiconductor device comprising:

a semiconductor substrate comprising a first main surface and a second main surface opposite to said first main surface;

a first strain relief plate comprising a bottom surface which is in contact with said first main surface of said semiconductor substrate; and

a second strain relief plate comprising a top surface which is in contact with said second main surface of said semiconductor substrate,

wherein said semiconductor substrate includes:

a first semiconductor layer of a first conductivity type comprising a first bottom surface and a first top surface opposite to said first bottom surface, said first bottom surface forming said second main surface of said semiconductor substrate;

a second semiconductor layer of a second conductivity type comprising a second bottom surface and a second top surface opposite to said second bottom surface, said second bottom surface including an interface with said first top surface of said first semiconductor layer;

a third semiconductor layer of said first conductivity type comprising a third bottom surface and a third top surface opposite to said third bottom surface, said third bottom surface including an interface with said second top surface of said second semiconductor layer; and

a second main electrode which is formed on the whole of said first bottom surface of said first semiconductor layer and is in direct mechanical contact with said top surface of said second strain relief plate,

a plurality of protruding portions are arranged radially and circumferentially about said semiconductor substrate on said first main surface of said semiconductor substrate,

each of said plurality of protruding portions comprises a fourth semiconductor layer of said second conductivity type,

said fourth semiconductor layer comprises a fourth bottom surface and a fourth top surface opposite to said fourth bottom surface, said fourth bottom surface and a corresponding region out of said third top surface of said third semiconductor layer forming a pn junction,

said fourth top surface forms a top surface of a corresponding one out of said plurality of protruding portions;

said pn junction is located within said corresponding one of said plurality of said protruding portions,

a top surface of each of first protruding portions belonging to at least one group out of a first group of outermost protruding portions and a second group of innermost protruding portions is entirely covered with a first insulating layer, said outermost protruding portions located most outward in a radial direction out of said plurality of protruding portions, said innermost protruding portions located most inward in said radial direction out of said plurality of protruding portions,

a first clearance constantly exists between a top surface of said first insulating layer and a first region of said bottom surface of said first strain relief plate which is located immediately above said top surface of said first insulating layer,

a first main electrode is formed on a top surface of each of said plurality of protruding portions except said outermost protruding portions and said innermost protruding portions,

said first main electrode is in direct mechanical contact with said bottom surface of said first strain relief plate,

said first main surface of said semiconductor substrate includes an exposed surface of said fourth semiconductor layer for each of said plurality of protruding portions and exposed regions of said third top surface, and

a control electrode is formed as one pattern on a region of said first main surface in which no surface of said plurality of protruding portions is included.

Claim 2 (Original): The pressure contact type semiconductor device according to claim 1,

wherein a top surface of each of second protruding portions belonging to the other group out of said first group and said second group is entirely covered with a second insulating layer, and

a second clearance constantly exists between a top surface of said second insulating layer and a second region of said bottom surface of said first strain relief plate which is located immediately above said top surface of said second insulating layer.

Claim 3 (Original): The pressure contact type semiconductor device according to claim 2,

wherein each of said outermost and innermost protruding portions is smaller in size than any other one of said plurality of protruding portions.

Claim 4 (Original): The pressure contact type semiconductor device according to claim 2,

wherein said outermost protruding portions are continuous with one another to form a single ring extending along an entire circumference of said semiconductor substrate.

Claim 5 (Currently Amended): A pressure contact type semiconductor device comprising:

a semiconductor substrate comprising a first main surface and a second main surface opposite to said first main surface;

a first strain relief plate comprising a bottom surface which is in contact with said first main surface of said semiconductor substrate; and

a second strain relief plate comprising top surface which is in contact with said second main surface of said semiconductor substrate,

wherein said semiconductor substrate includes:

a first semiconductor layer of a first conductivity type comprising a first bottom surface and a first top surface opposite to said first bottom surface, said first bottom surface forming said second main surface of said semiconductor substrate;

a second semiconductor layer of a second conductivity type comprising a second bottom surface and a second top surface opposite to said second bottom surface, said second bottom surface including an interface with said first top surface of said first semiconductor layer;

a third semiconductor layer of said first conductivity type comprising a third bottom surface and a third top surface opposite to said third bottom surface, said third bottom

surface including an interface with said second top surface of said second semiconductor layer; and

a second main electrode which is formed on the whole of said first bottom surface of said first semiconductor layer and is in direct mechanical contact with said top surface of said second strain relief plate,

a plurality of protruding portions are arranged radially and circumferentially about said semiconductor substrate on said first main surface of said semiconductor substrate,

each of said plurality of protruding portions comprises a fourth semiconductor layer of said second conductivity type,

said fourth semiconductor layer comprises a fourth bottom surface and a fourth top surface opposite to said fourth bottom surface, said fourth bottom surface and a corresponding region out of said third top surface of said third semiconductor layer forming a pn junction,

said fourth top surface forms a top surface of a corresponding one out of said plurality of protruding portions;

said pn junction is located within said corresponding one of said plurality of said protruding portions,

a first main electrode is formed on a top surface of each of said plurality of protruding portions,

said first main electrode which is formed on a top surface of each of first protruding portions belonging to at least one group out of a first group of outermost protruding portions and a second group of innermost protruding portions, is constantly not in mechanical contact with said bottom surface of said first strain relief plate, said outermost protruding portions located most outward in a radial direction out of said plurality of protruding portions, said

innermost protruding portions located most inward in said radial direction out of said plurality of protruding portions,

said first main electrode, which is formed on said top surface of each of said plurality of protruding portions, except said outermost and innermost protruding portions, is in direct mechanical contact with said bottom surface of said first strain relief plate,

said first main surface of said semiconductor substrate includes an exposed surface of said fourth semiconductor layer for each of said plurality of protruding portions and exposed regions of said third top surface, and

a control electrode is formed as one pattern on a region of said first main surface in which no surface of said plurality of protruding portions is included.

Claim 6 (Original): The pressure contact type semiconductor device according to claim 5,

wherein said first main electrode which is formed on a top surface of each of second protruding portions belonging to the other group out of said first and second groups is constantly not in contact with said bottom surface of said first strain relief plate.

Claim 7 (Currently Amended): The pressure contact type semiconductor device according to claim 6,

wherein said first strain relief plate is an annular member which comprises an inner peripheral surface and an outer peripheral surface,

said first strain relief plate includes:

a first missing portion provided in a first corner portion thereof at which said bottom surface, and said outer peripheral surface of said first strain relief plate meet each other; and

a second missing portion provided in a second corner portion thereof at which said bottom surface and said inner peripheral surface of said first strain relief plate meet each other,

a first clearance constantly exists between said first main electrode on each of said outermost protruding portions and said first missing portion located immediately above said first main electrode on each of said outermost protruding portions, and

a second clearance constantly exists between said [[fist]] first main electrode on each of said innermost protruding portions and said second missing portion located immediately above said first main electrode on each of said innermost protruding portions.

Claim 8 (Canceled).

Claim 9 (Canceled).